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SPECIFICATION

1. Title of the Invention

LIQUID-CRYSTAL ELECTROOPTICAL DEVICE

2. Claims

1. A liquid crystal electrooptical device in which a liquid crystal display device and a charge storage capacitor are connected in parallel with an insulated gate field effect semiconductor device characterized in that

said liquid crystal display device has one electrode formed on said insulated gate field effect semiconductor device.

2. A liquid crystal electrooptical device according to claim 1, characterized in that one electrode of the liquid crystal display device is so formed as to prevent light from irradiating on the insulated gate field effect semiconductor device.

3. Detailed Description of the Invention

The present invention relates to a liquid crystal electrooptical device having vertical-channel, insulated gate semiconductor device laminated on a substrate.

The present invention also relates to a liquid crystal

electrooptical device having composite semiconductor devices having capacitors connected with a source or a drain of the insulated gate field effect semiconductor devices laminated on a substrate.

The present invention is characterized by providing a liquid crystal display type display device consisting of such composite semiconductor devices arranged in matrix structure on a substrate.

In the case of providing a flat solid state display device, a liquid crystal display device wherein electrodes are formed within parallel glass plates and a liquid crystal is injected between these electrodes is well known in the present invention. In this case, however, the maximum number of pixels on the display portion is limited to 20 to 200. Where more pixels are formed, necessary terminals brought out from the display device should be equal in number with the pixels. Hence, this display structure has not been put into practical use at all. Accordingly, it is necessary that the display portion is made up of plural pixels arranged in matrix structure and to control any desired pixel and turn on or off it, a field effect semiconductor device (referred to as IGF) corresponds to each such pixel. A control signal is supplied to the IGF to turn on or off the corresponding pixel.

This liquid crystal display portion can be represented in terms of a capacitor (hereinafter referred to as abbreviated C) as an equivalent circuit. Therefore, such IGF and C are arranged in a 2 × 2 matrix structure(40), for example, is shown in Fig. 1.

Referring to Fig. 1, one IGF (10) and one C (31) form one pixel in the matrix (40). This is used in a column and connected with

(51) and (51') and with bit lines. On the other hand, gates are connected to form columns (41) and (41').

It is assumed that (51) and (41) take state "1" and that (51') and (41') take state "0". Only address (1,1) is selected and turned on. A liquid crystal display portion that is electrically equivalently represented by C (31) can be selectively turned on. The present invention is intended to form other insulated-gate semiconductor devices (50), other inverters (60), and resistors (70) on the same substrate to form decoders and drivers on the same substrate.

Thus, by combining the invention with their design specifications, a solid-state display device that is adapted for a flat TV and can replace a cathode ray tube for a TV set has been successfully fabricated.

Further, a display device for a calculator needs only 10^2 to 10^3 pixels. For a TV, 10^4 to 10^5 (e.g., 25×10^3) pixels are formed on the same substrate, and necessary peripheral decoders and drivers may be simultaneously formed using IGF devices, inverters, and resistors.

The present invention relates to pixels at which lamination type IGF devices necessary for fabrication of such a system and liquid crystal display portions are connected.

Fig. 2 is a vertical cross section of a laminated type IGF in accordance with the present invention and illustrates the fabrication process.

In the figure, on an insulating substrate, for example, a glass

or an alumina substrate a first semiconductor (2) of P^+ or N^+ conductivity type (hereinafter simply referred to as the S1), an insulating or semi-insulating film (3) having a thickness that can pass a tunnel current, a second semiconductor (4) of intrinsic, N type, or P type (hereinafter simply referred to as the S2), and a third semiconductor (5) (hereinafter simply referred to as the S3) having the same conductivity type as the first semiconductor are laminated.

These semiconductors are deposited on the substrate at a temperature of room temperature to 500°C by making use of glow discharge of silane. Amorphous or semi-amorphous silicon semiconductors are used. The description of the present invention centers on semi-amorphous semiconductor (hereinafter simply referred to as SAS). Detailed examples of the SAS are described, for example, in patent applications of the present Applicant, e.g., Japanese Patent Application No. 143885/1980, filed October 15, 1980, entitled "Semi-amorphous Semiconductor", Japanese Patent Application No. 122786/1980, filed September 4, 1980, entitled "Semiconductor Device", and Japanese Patent Application No. 026388/1980, filed March 3, 1980, entitled "Semi-amorphous Semiconductor".

Referring still to Fig. 2, the S3 is selectively removed by photolithography technique. Using this S3 as a mask, the S2 is removed. To check the ending point of this photoetching, an insulating or semi-insulating film (hereinafter simply referred to as the insulating film) (13) is made of silicon nitride.

The thickness is as thin as 5 to 30 Å and it is formed by exposing the first semiconductor to an ammonia atmosphere that is plasma-irradiated. Then, this insulating film (13) is chemically removed to obtain the result shown in Fig. 2(B).

To make a subsequently formed insulating film on the S3 thicker, a silicon oxide film having a thickness of 0.3 to 1 μ may be previously formed by LPCVD (low-pressure chemical vapor deposition). Mo or W is deposited on the S3 to a thickness of 0.2 to 0.5 μ. Furthermore, SiO_2 is deposited on it to a thickness of 0.3 to 1 μ, thus enhancing the conductivity of the S3. This is effective in achieving a matrix structure.

Moreover, in Fig. 2(B), the side surfaces may be formed vertical to the surface of the substrate (1). Where a trapezoid is taper-etched to make it unnecessary to remove the portions of later laminated gate electrodes that lie over step portions, the process is made efficient.

Furthermore, as shown in Fig. 2(C), the S1 is shaped into an arbitrary given shape by photolithography technique. In the figure, the substrate surface is exposed at (11).

Then, an insulating film (6) is formed on the whole surfaces of the S1, S2, and S3. This insulating film is activated by electromagnetic energy having a frequency of 13.56 MHz to 2.45 GHz. The insulating film is immersed in an atmosphere of oxygen or a mixture gas of oxygen and hydrogen at 100 to 700°C and oxidized.

In addition, silicon nitride or phosphosilicate glass may be formed by LPCVD to form a multilayer structure.

This insulator (16) is deposited as a gate insulator (16) around the sides of the S2 (14). The surfaces of the S1 and S3 can be formed as isolation films.

As indicated in (D), electrode holes (8) and (7) are formed in the S1 (12) and S3(15), respectively, by a third photolithography technique. Another metal or semiconductor layer connected with the gate electrodes is deposited.

This film is selectively etched by a fourth photolithographic technique to form a gate electrode (17) in two directions together with gate insulators (16) and (16'). Simultaneously, the film is wired to other IGF devices, capacitors, and resistors via the electrode holes from the S1(12) and S3(15) in an intimate relation to the substrate surface or to the insulator (6).

Fig. 2(E) is obtained by viewing the cross section of Fig. 2(D) from a side of A-A'. Respective reference numerals of Fig. 2(E) are corresponding to that of Fig. 2(D).

Semiconductors in accordance with the present invention are mostly semi-amorphous semiconductors (SAS devices). Hydrogen is used to neutralize dangling bonds in the SAS devices. The substrate, the semiconductors, and the electrode leads are made of different materials. To reduce the stress induced by thermal expansion of these materials, all the processing steps should be carried out at 300-600°C or below, preferably below 300°C.

The gate electrode (17) may have a multilayer wiring structure such as a double structure of a semiconductor having the same conductivity type as the S1 and S3, and the metal such as Mo.

In this way, the source or drain is formed from the S1(12). The channel formation region (9), (9') is formed from the S2(14). The drain or source is formed from the S3(15). Gate insulator (16), (16') is deposited on the side surfaces of the channel formation region. The gate electrode (17) is formed on its outer side surfaces. In this way, a lamination type IGF (10) can be built.

In this invention, it is determined by the thickness of the channel length S2(14). In this example, it is set to 0.05 to 0.5 μ. The mobility of the SAS is different from that of a single crystal and only 1/5 to 1/100 of that of a single crystal. Therefore, by shortening the channel length, the characteristics of the IGF are improved.

The electron bulk mobility of the semi-amorphous silicon (SAS) is 100 to 500 cm^2 V/s, that is, 1/3 to 1/10. On the other hand, the hole mobility is 5 to 100 cm^2 V/s, that is, 1/5 to 1/100. However, where it is considered that the electron mobility of amorphous silicon is 0.1 to 10 cm^2 V/s and that the hole mobility is greater by a factor of 10 to 10^3 compared with 0.01 cm^2 V/s or less, it is quite important to use SAS having microcrystallite structure in the semiconductor device in accordance with the present invention.

In the IGF in accordance with the present invention, the electron mobility is greater than 3 times that of a single crystal and 5 to 100 times the hole mobility. Therefore, it is quite desirable to make the device the N-channel type.

Since an intrinsic semiconductor whose surface is not doped with impurities is N^- type, it is used as P type in the S2.

Fig. 3 is a vertical cross section of another IGF in accordance with the present invention and illustrates the fabrication steps.

In Fig. 3(A), a silicon film of semi-amorphous silicon (SAS) is formed as S1(2) on a substrate (1). The film is selectively etched by photolithography technique to expose parts (11) of the substrate (1).

To crystallize the SAS, optical annealing (laser annealing), thermal annealing, or a combination of them is used to change the SAS into a single crystal or polycrystalline structure. The heating temperature is set to lower than 700°C to prevent the substrate material from undergoing thermal stress.

It is only necessary that this S1(2) be fundamentally different from the S2 and S3 in etching rate. Therefore, the S1 can be an intrinsic or semi-insulating semiconductor to which P or N type oxygen or nitrogen is added and which has stoichiometry given by SiO_{2-x} ($0.5 < x < 2$) or Si_3N_{4-x} ($1 < x < 4$).

As shown in Fig. 3(B), S2(4) is then formed on the upper surface as intrinsic, N^- type, or P type and S3(5) is formed on it as the same conductivity type (P type or N type) as S1 within the same reaction furnace.

Furthermore, as shown in Fig. 3(C), these S2(4) and S3(5) are shaped substantially identically; the other portions are selectively removed. In this way, S2(14) and S3(15) are formed on S1(12). Thereafter, upper surfaces of the S1, S2, and S3 are oxidized to form an insulating film (6). At this time, the vicinities of the side surfaces of the S2(14) are formed as a gate insulating

film (16). The other portions are formed as an isolation film.

Then, a film of a semiconductor or conductor is formed over the whole surface using the electrode holes or contact portions (7) and (8) by a third photolithography technique. This film is selectively removed by a fourth photolithography technique to form electrode leads (22) continuous with the other portions on the S1(12) and similar electrodes and leads on the S3(15) via the contacts (7). A gate electrode (17) is formed on gate electrodes (16), (16') at the side surfaces of channel formation regions (9), (9') in the vicinities of the side surfaces of the S2(14).

In this manner, the source or drain is formed from the S1(12). The channel formation regions (9), (9') are formed from the S2(14). The drain or source is formed from the S3(15). The gate is made up of a gate insulator (16), (16') and the gate electrode (17). It is assumed that the gate electrode is set to "1" and that the source or drain is set to "1". Where a current flows through the channel formation regions, an ON state can be created. If one or both are "0", an OFF state can be created.

In the N-channel IGF, "1" means a positive current of 0.5 to 10 V, and "0" means 0 V or a current lower than the threshold voltage.

As for a P-channel IGF, the polarities of the electrodes may be varied. The logics is the same for Figs. 1 and 2 and for Fig. 3 that will be described below and for the examples of the present invention.

The resistor (70) of Fig. 1 is determined by the resistivity of the bulk component of the S2 independent of the voltage applied

to the gate in Figs. 2(D), (E), and 3(D). That is, the S1, S2, and S3 may be laminated without providing the gate electrode. The resistance value may be determined according to the resistivity of the S2, its thickness, and the area occupied on the substrate in accordance with the design specifications.

The inverter (60) of Fig. 1 has a driver (61) designed as shown in Figs. 2 and 3(D). Its load (64) is an enhancement or depletion type IGF that is connected with one of S3(15) and S1(12) and with the gate electrode (17).

The output of this inverter (60) is indicated by (62). Two IGF devices are laminated on this substrate and spaced from each other. In this way, a composite structure is fabricated. The input portion may be formed so as to correspond to the gate electrode (17).

Fig. 4(A) is a vertical cross section of other structure in accordance with the present invention. That is, formed on a substrate (1) are S1(12), S2(14), S3(15), and an IGF (10) whose gate portion is made of a gate insulator (16) and a gate electrode (17). Other portion made of S1(12) and connected with an electrical system forms one electrode 22 of a capacitor. This other portion also forms the other electrode 32 of a liquid crystal display. That is, the S1 forms one electrode of two capacitors. One of the capacitors is designed to have a large storage capacitance, for prolonging the display time of the liquid crystal display.

Namely, in Fig. 1, even if a certain IGF is retained in ON state for 10 to 100 nsec, the liquid crystal display can be given

so-called persistence characteristics which provides a display for as long as 1 to 1000 ms because the liquid-crystal panel and the capacitors are connected in parallel. Where the storage capacitor is large in this way, a vivid display can be provided on a flat panel comparable to a CRT for TV. Also, the number of pixels is 10^4 to 10^5. If they are scanned digitally, "0" and "1" can be kept displayed on other pixels. Where the number of pixels is more than 10, the storage capacitor is effective in preventing the viewer's eye from getting tired.

Because this storage capacitor and the gate insulator 16 are made of the same material, capacitors of this kind can be manufactured by batch processing without needing any additional process step. To increase the capacitance with a small area, silicon nitride, tantalum oxide, or other ferroelectric substance may be used rather than silicon oxide.

Other electrodes (32) electrically connected with the S1(12) in accordance with the present invention are formed via electrode holes (25). An interlayer insulator such as polyimide or PIQ is deposited to a thickness of 1 to 3 μ on these IGF devices 10 . It is selectively etched photolithography technique. Each electrode (32) determines the size of one pixel. In a calculator or the like, it has a diameter of 0.1 to 5mmϕ or rectangle. In the scanning type as shown in Fig. 1, a matrix construction of 500 × 500, each with 1 to 50 μ□, is formed. A liquid-crystal display portion (31) is fabricated by forming a first plate consisting of semiconductor device electrodes formed on the substrate, preparing a glass plate

(28) having a transparent electrode (27) as made of ITO as a second plate, placing these two plates with a gap of 1 to 20 μm therebetween, and injecting a nematic liquid crystal (26), for example, in the gap.

Furthermore, the display may be designed to provide colors. For example, three layers of pixels may be overlapped. The three elements of red, green, and blue are alternately arranged.

In Fig. 4(A), a storage capacitor and a liquid crystal that is represented by a liquid-crystal capacitor in an equivalent circuit are connected in parallel. In contrast, in Fig. 4(B), they are placed in series.

Specifically, on one electrode (22) which is electrically connected with the S1(12), a dielectric film (23), another electrode (24), one electrode(32)of a second liquid crystal capacitor (31) connected with the electrode (24) are connected with each other via openings (25). In correspondence with the electrode(32), a counter electrode (27) made of a transparent electrode is provided with a dielectric of the liquid crystal (26)interposed therebetween.

As can be seen from Figs. 4(A) and (B), the present invention is characterized in that plural IGF capacitors and resistors are formed on the substrate (1). At the same time, a flat panel of a liquid crystal display is formed with a sandwich structure on the substrate(1).

Further, as can be seen from the figures, where light is irradiated from above, the light would normally fall on the IGF(10), causing leakage in state "0". To prevent this, an upper cover is

mounted, and one electrode (32) of each pixel is formed. This constitutes a distinct feature.

In addition, as a great feature, i.e., differently from the prior art structure, lamination type IGF is provided on the insulating substrate and completely isolated from other pixels. The whole process step is carried out at a temperature of 600°C or lower, especially 300°C or lower. If this panel has a large area, it is less affected by thermal strain.

As another feature of the invention, semiconductors used in the present invention are mostly non-single-crystal semiconductor. Especially, semi-amorphous semiconductor (SAS) assumes an intermediate structure between amorphous and single crystal structure and is stable to thermal energy up to 600°C.

Especially, SAS is a non-single-crystal structure having lattice distortion having large microcrystallite structure of 10 to 100 Å. During the fabrication, if an inductive energy of 500 kHz to 3 GHz is used, it is sufficient to elevate the temperature to 300°C. In addition, the physical characteristics of the SAS are such that the diffusion lengths of electrons and holes are greater than that of amorphous silicon by a factor of 100 to 10^5. Such a non-single-crystal semiconductor is laminated on a substrate. IGF devices are formed. Electrical currents flow through them vertically. Therefore, microchannel IGF devices having channel lengths of 0.1 to 1 μ can be fabricated without using accurate photolithography techniques.

As a still other feature of the invention, in view of the

characteristics of the SAS, the threshold voltage V_{TH} of the IGF is controlled by the dopant concentration in the S2 and by the applied RF power rather than by ion implantation, for example.

Therefore, the withstand voltage can be controlled within a range of 20 to 30 V. V_{TH} can be controlled from -4 to 4 V within a range of ± 0.2 V. Furthermore, 1/5 to 1/50 of conventional single-crystal insulated-gate semiconductor device can be obtained in spite of the fact that non-single-crystal semiconductor is used, because the frequency characteristics are microchannels having channel lengths of 0.1 to 1 μ.

Where silicon nitride having a thickness of 10 to 40 Å is inserted between the S1 and S2 as shown in Fig. 1, the leakage (although it is a reverse leakage) from this N^+-P junction or from P^+-N junction is less than 10 mA if 10V is applied in the reverse direction. This is comparable to reverse leakage from a single crystal and is desirable.

Where 10 to 30 mol% of oxygen, for example, is added to the S1, the reverse leakage is similarly low in the structure shown in Fig. 3. The amount of leakage is only 1/10 to 1/10 of the amount of leakage occurring in an undoped structure. Of course, this low leakage is quite advantageous where the matrix structure shown in Fig. 1 is implemented.

Where the laminated S1, S2, and S3 are all made of amorphous silicon semiconductor, the reverse leakage is more than 1 mA when a reverse bias of 10 V is applied. Where they are made of SAS, the reverse leakage is reduced to 5 to 50 nA, for the following reason.

The dopants such as B or P in the P- or N-type semiconductor of S1 or S3 reside in substitutional sites. The ionization rate is 4 N or more in the same way as a single crystal. The activation energy is 0.005 to 0.001 eV, which is smaller than the activation energy of 0.2 to 0.3 eV of amorphous semiconductor.

Therefore, the impurities which have once coordinated do not diffuse out of the laminated layers. As a result, a clean junction is formed.

That is, the features of the present invention are as follows. Lamination type IGF devices are provided. Non-single-crystal semiconductors are used in them. Especially, SAS is employed. To make clear the junction between S1 and S2, nitrogen oxide is added to the S1 to enhance the reverse withstand voltage mainly as an energy bandwidth. Alternatively, an SIS junction in which an insulating or semi-insulating film is placed between other layers is formed.

For such lamination type IGF devices, accurate photolithography techniques as used conventionally is not employed. However, plural IGF devices, resistors, and capacitors are fabricated on a substrate, especially on an insulating substrate. This structure can be extended to a liquid-crystal display.

In the present invention, silicon is used as a semiconductor, and silicon oxide or silicon nitride is used as an insulator. However, germanium, InP, BP, GaAs, or the like may also be used as a semiconductor. A single-crystal semiconductor may be used instead of the non-single-crystal semiconductor. Furthermore, it is obvious

that polycrystalline semiconductor having large crystal grain diameters may be used instead of SAS.

4. Brief Description of the Drawings

Fig. 1 shows an equivalent circuit of a matrix structure using pixels consisting either of insulated gate semiconductor devices, inverter resistors, and capacitors or of insulated-gate semiconductor devices and capacitors for use in a liquid-crystal electrooptical device in accordance with the present invention;

Figs. 2 and 3 are vertical cross sections illustrating the process for laminated insulated gate semiconductor devices for use in a liquid crystal electrooptical device in accordance with the present invention; and

Fig. 4 is a vertical cross section of a composite semiconductor showing a flat display in which laminated insulated gate semiconductor devices in accordance with the invention, capacitors, and a liquid crystal are integrated.